

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Balram, et al.

Serial No.: 09/127,117

Patent No: 6,034,733

Filed: July 29, 1998

Confirmation No.: 9734

Group Art Unit: 2711

Examiner: Kostak, Victor R.

Issue Date: March 7, 2000

Attorney Ref. 250839-1720

For: Timing and Control for Deinterlacing and Enhancement of Non-Deterministically Arriving Interlaced Video Data

PETITION FOR DUPLICATE LETTERS PATENT

**Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450**

Attention Nancy Johnson:

The undersigned hereby petitions for a duplicate copy of the original letters patent in connection with the above-referenced patent.

NOTE: A similar petition has already been filed and approved in connection with U.S. Patent 6,473,082 (serial no. 09/313,857). Also, duplicate petitions (to the present petition are being filed in the following matters (as the patents listed below were lost under similar circumstances to that of the present patent):

| Patent No. | Serial No. | Title |
|-------------------|-------------------|------------------------------------------------------------------------------------|
| 6,405,267 | 09/236,062 | Command Reordering for Out of Order Bus Transfer |
| 5,777,590 | 08/519,690 | Grayscale Shading for Liquid Crystal Display Panels |
| 5,910,820 | 08/621,567 | Correction of Flicker Associated with Noninterlaced to Interlaced Video Conversion |

| Patent No. | Serial No. | Title |
|-------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------|
| 5,956,431 | 08/942,860 | System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values |
| 6,658,146 | 09/351,930 | Fixed-Rate Block-Based Image Compression with Inferred Pixel Values |
| 5,517,626 | 08/011,449 | Open High Speed Bus for Microcomputer System |
| 5,778,096 | 08/489,488 | Decompression of MPEG Compressed Data in A Computer System |
| 5,774,676 | 08/538,887 | Method and Apparatus for Decompression of MPEG Compressed Data in a Computer System |
| 5,818,967 | 08/490,322 | Video Decoder Engine |
| 5,977,933 | 08/585,135 | Dual Image Computer Display Controller |
| 5,757,670 | 08/508,636 | Frame Reconstruction for Video Data Compression |
| 6,476,808 | 09/419,699 | Token-Based Buffer System and method for a Geometry Pipeline in Three Dimensional Graphics |
| 5,416,749 | 08/165,035 | Improved Data Retrieval From Sequential-Access memory Devices |
| 6,052,133 | 08/884,361 | Multi-Function Controller and Method for a Computer Graphics Display System |
| 5,883,675 | 08/676,527 | Close Captioning Processing Architecture for Providing Text Data During Multiple Fields of a Video Frame |
| 5,914,719 | 08/753,923 | Index and Storage System for Data Provided in the Vertical Blanking Interval |
| 5,764,240 | 08/629,784 | Method and Apparatus for Correction of Video Tearing Associated with a Video Graphics Shared Frame Buffer, As Displayed on a |

| Patent No. | Serial No. | Title |
|-------------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| | | Graphics Monitor |
| 5,852,451 | 08/780,787 | Pixel Reordering for Improved Texture Mapping |
| 5,990,912 | 08/884,573 | Virtual Address Access to Tiled Surfaces |
| 5,990,965 | 08/942,143 | System and Method for Simultaneous Flicker Filtering and Overscan Compensation |
| 5,852,568 | 08/788,391 | System and Method for a Fast Carry/Sum Select Adder |
| 5,856,947 | 08/920,604 | Integrated DRAM with High Speed Interleaving |
| 6,084,568 | 08/969,637 | System and Methods for 2-Tap and 3-Tap Flicker Filtering of Non-Interlaced Computer Graphics to Interlaced Lines for Television Display |
| 5,945,997 | 08/883,536 | Block- and Band-Oriented Traversal in Three-Dimensional Triangle Rendering |
| 6,031,258 | 09/036,351 | Hi DC Current and Stagger Power/Ground Pad |
| 5,948,083 | 08/941,402 | System and Method for a Self-Adjusting Data Strobe |
| 5,958,038 | 08/966,904 | Computer Processor and Method for Data Streaming |
| 6,009,019 | 09/019,345 | Real Time DRAM Eliminating a Performance Penalty for Crossing a Page Boundary |
| 6,008,794 | 09/021,718 | Flat-Panel Display Controller with Improved Dithering and Frame Rate Control |
| 6,041,419 | 09/085,984 | Programmable Delay Timing Calibrator for High Speed Data Interface |
| 5,935,198 | 08/755,545 | Multiplier with Selectable Booth Encoders for Performing 3D Graphics Interpolations with Two Multiplies in a Single Pass Through the Multiplier |

| Patent No. | Serial No. | Title |
|-------------------|-------------------|--------------------------------------------------------------------------------------------------------------|
| | | |
| 6,005,412 | 09/057,047 | AGP/DDR Interfaces for Full Swing and Reduced Swing (SSTL) Signals on an Integrated Circuit Chip |
| 6,011,565 | 09/057,628 | Non-Stalled Requesting Texture Cache System and Method |
| 6,154,195 | 09/079,973 | System and Method for Performing Dithering with a Graphics Unit Having an Oversampling Buffer |
| 6,144,365 | 09/060,923 | System and Method for Performing Blending Using an Oversampling Buffer |
| 5,848,264 | 08/740,248 | Debug and Video Queue for Multi-Processor Chip |
| 6,034,733 | 09/127,117 | Timing and Control for Deinterlacing and Enhancement of Non-Deterministically Arriving Interlaced Video Data |
| 5,402,513 | 08/266,164 | Video Window Generator with Scalable Video |
| 5,581,279 | 08/147,456 | VGA Controller Circuitry |
| 5,440,683 | 08/328,382 | Video Processor Multiple Streams of Video Data in Real-Time |
| 5,757,347 | 08/061,802 | Process for Producing Shaded Colored Images Using Dithering Techniques |
| 5,889,499 | 08/683,102 | System and Method for the Mixing of Graphics and Video Signals |
| 5,625,379 | 08/402,935 | Video Processing Apparatus, System and Methods |
| 5,521,614 | 08/235,827 | Method and Apparatus for Expanding and Centering VGA Text and Graphics |
| 5,821,918 | 08/402,862 | Video processing Apparatus System and Methods |

| Patent No. | Serial No. | Title |
|-------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 5,734,362 | 08/474,416 | Brightness Control for Liquid Crystal Displays |
| 5,828,383 | 08/576,870 | Controller for Processing Different Pixel Data Types Stored in the Same Display Memory By Use of Tag Bits |
| 5,005,546 | 08/619,203 | Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder |
| 5,793,386 | 08/672,620 | Register Set Reordering for a Graphics Processor Based Upon the Type of Primitive to be Rendered |
| 5,758,128 | 08/673,774 | Object Referenced Memory Mapping |
| 5,977,960 | 08/707,937 | Apparatus, Systems, and Methods for Controlling Data Overlay in Multimedia Data Processing and Display Systems Using Mask Techniques |
| 5,875,295 | 08/724,618 | Instruction Format for Ensuring Safe Execution of Display List |
| 6,088,016 | 08/777,557 | Dithering Method and Apparatus Using Ramp Probability Logic |
| 6,008,796 | 08/856,546 | Software-Based Dithering Method and Apparatus Using RAMP Probability Logic |
| 5,841,443 | 08/803,460 | Method for Triangle Subdivision in Computer Graphics Texture Mapping to Eliminate Artifacts in High Perspective Polygons |
| 5,977,983 | 08/803,461 | Method and Apparatus for Adjusting Graphics Processing Procedures Based on a Selectable Speed/Quality Gauge |
| 6,072,508 | 08/818,053 | Method and Apparatus for Shortening Display List Instructions |
| 6,028,613 | 08/821,125 | Method and Apparatus for Programming a Graphics Subsystem Register Set |

| Patent No. | Serial No. | Title |
|-------------------|-------------------|----------------------------------------------------------------------------------------------------------------------|
| 5,835,104 | 08/841,360 | Variable Band Size Compositing Buffer Method and Apparatus |
| 6,141,020 | 08/968,309 | Opposing Directional Fill Calculators in a Graphics Processor |
| 6,115,507 | 09/076,670 | Method and Apparatus for Upscaling Video Images in a Graphics Controller Chip |
| 6,128,026 | 09/122,422 | Double Buffered Graphics and Video Accelerator Having a Write Blocking Memory Interface and Method of Doing the Same |
| 6,683,978 | 09/442,114 | System and Method for Fixed Rate Block-Based Image Compression with Inferred Pixel Values |
| 6,999,077 | 10/855,992 | Z-Buffer Based Interpenetrating Object Detection For Antialiasing |

The original patent was received by S3 Incorporated. S3 Incorporated later changed its name to SonicBlue Incorporated, and SonicBlue Incorporated assigned its interests in this patent to S3 Graphics Co., Ltd. These transfers are reflected in the assignment records of the Patent Office.

Through these various transfers, official patent files have similarly been transferred around and the original letters patent has been lost from the files. In fact, numerous patent files were involved in these transfers (not merely this single patent file), and representatives of the current owner have discovered that a number of the files they received are missing the original letters patents. The owner has made requests of counsel for the previous owners, and counsels have confirmed that the original patents are not in their files. This application is one of the matters for which the original letters patent has been lost.

Therefore, the undersigned hereby petitions the PTO to re-print a duplicate copy of the original letters patent for U.S. patent No 6,034,733.

A credit card authorization is provided herewith to cover this petition fee. Any additional fee that may be required is hereby authorized to be charged to deposit account No. 20-0778.

Respectfully submitted,
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